AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims for this application:

Listing of Claims:

1. (Currently amended) A method for measuring the registration between at least two integrated circuit layers, one residing over the other, said method comprising:

generating a top-down image of a field of said at least two integrated circuit layers, each of said layers having a respective visible feature in said image;

digitizing said image and processing said digitized image to determine a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers;

determining a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location, wherein at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers; and

determining if said relative location is within stored acceptable design limits for said integrated circuit layers by comparing said relative location to said stored acceptable design limits.

Claim 2 (Canceled).

3. (Previously presented) The method of claim 1, wherein said step of determining said location of said first feature reference point in said visible feature of one of said layer includes determining an x-axis value, X_1, and an y-axis value, Y_1.

4. (Previously presented) The method of claim 1, wherein said step of determining said location of said second feature reference point in said visible feature of another of said layer includes determining an x-axis value, X_2, and an y-axis value, Y_2.

5. (Previously presented) The method of claim 1, wherein said step of determining said relative location further includes determining an x-axis value, Δx, and an y-axis value, Δy, where

$$\Delta x = X_1 - X_2$$

$$\Delta y = Y_1 - Y_2.$$

6. (Previously presented) The method of claim 1, wherein said step of determining if said relative location is within stored acceptable design limits includes comparing said relative location to a stored data having reference locations and tolerable limits.

7. (Previously presented) The method of claim 6 further including the step of calculating an offset value by calculating the difference in the positions of a first reference location and a second reference location.

8. (Original) The method of claim 7 further including the step of comparing said offset value to a predetermined tolerance.

9. (Original) The method of claim 1, wherein said step of generating said image of said field is produced by an imaging system.

10. (Original) The method of claim 9, wherein said imaging system includes a scanning electron microscope.

11. (Original) The method of claim 9, wherein said imaging system includes an optical system.

12. (Original) The method of claim 11, wherein said optical system comprises a microscope and a video camera.

13. (Original) The method of claim 1, wherein said integrated circuit layers are chosen from a group of integrated circuit layers consisting of semiconductor layers, dielectric layers, and photoactive layers.

14. (Currently amended) A system for measuring the registration between at least two integrated circuit layers, one residing over the other, said system comprising:

an imaging system for generating a top-down of a field of said at least two integrated circuit layers, each of said layers having a respective visible feature in said image;

means for digitizing said image and processing said digitized image to determine a location of a first feature reference point in said visible feature of one of said layers, and a location of a second feature reference point in said visible feature of the other of said layers, to indicate a relative location of said visible feature of one of said layers, relative to said visible feature of the other of said layers, wherein at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers; and

means for determining if said relative location is within acceptable design limits for said integrated circuit layers.

Claim 15 (Canceled).

16. (Previously presented) The system of claim 14, wherein said means for determining said location of said first feature reference point in said visible feature of one of said layer further determines an x-axis value, X_1, and an y-axis value, Y_1.

17. (Previously presented) The system of claim 14, wherein said means for determining said location of said second feature reference point in said visible feature of another of said layer further determines an x-axis value, X_2, and an y-axis value, Y_2.

18. (Previously presented) The system of claim 14, wherein said means for determining said relative location further determines an x-axis value, Δx, and an y-axis value, Δy, where

$$\Delta x = X_1 - X_2$$

$$\Delta y = Y_1 - Y_2.$$

19. (Original) The system of claim 14, wherein said means for determining if said relative location is within acceptable design limits further compares said relative location to a stored data having reference locations and tolerable limits.

20. (Original) The system of claim 19 further including means for calculating an offset value.

21. (Original) The system of claim 20, wherein said means for calculating said offset value further compares said offset value to a predetermined tolerance.

22. (Original) The system of claim 14, wherein said means for generating said image of said field is an imaging system.

23. (Original) The system of claim 22, wherein said imaging system includes a scanning electron microscope.

24. (Original) The system of claim 22, wherein said imaging system includes an optical system.

25. (Original) The system of claim 24, wherein said optical system comprises a microscope and a video camera.

26. (Original) The system of claim 14, wherein said integrated circuit layers are chosen from a group of integrated circuit layers consisting of semiconductor layers, dielectric layers, and photoactive layers.

27. (Currently amended) A method for measuring the registration between integrated circuit layers, said method comprising:

providing a first integrated circuit layer on a semiconductor substrate, said first integrated circuit layer comprising at least a first visible feature;

providing a second integrated circuit layer over said first integrated circuit layer, said second integrated circuit layer comprising at least a second visible feature;

generating a top-down image of a field of said first and second integrated circuit layers, including said first and second visible features;

digitizing said top-down image to provide a digitized image, and processing said digitized image to determine a relative location of said first visible feature of said first integrated circuit layer, relative to said second visible feature of said second integrated circuit layer by determining a location of a first feature reference point in said first visible feature of said first integrated circuit layer, and a location of a second feature reference point in said second visible feature of said second integrated circuit layer to indicate said relative location, wherein at least one of said visible features is a non-metrological structure on said one of said integrated circuit layers; and

determining if said relative location is within stored acceptable design limits for said first and second integrated circuit layers by comparing said relative location to said stored acceptable design limits.

Claim 28 (Canceled).

29. (Previously presented) The method of claim 27, wherein said step of determining said location of said first feature reference point in said visible feature of said first integrated circuit layer includes determining an x-axis value, X_1, and an y-axis value, Y_1.

30. (Previously presented) The method of claim 29, wherein said step of determining said location of said second feature reference point in said visible feature of said second integrated circuit layer includes determining an x-axis value, X_2, and an y-axis value, Y_2.

31. (Previously presented) The method of claim 30, wherein said step of determining said relative location further includes determining an x-axis value, Δx, and an y-axis value, Δy, where

$\Delta x = X_1 - X_2$

$\Delta y = Y_1 - Y_2$.

32. (Previously presented) The method of claim 27, wherein said step of determining if said relative location is within stored acceptable design limits includes comparing said relative location to a stored data having reference locations and tolerable limits.

33. (Previously presented) The method of claim 32 further including the step of calculating an offset value by calculating the difference in the positions of a first reference location and a second reference location.

34. (Previously presented) The method of claim 33 further including the step of comparing said offset value to a predetermined tolerance.

35. (Previously presented) The method of claim 27, wherein said step of generating said top-down image of said field is produced by an imaging system.

36. (Previously presented) The method of claim 35, wherein said imaging system includes a scanning electron microscope.

37. (Previously presented) The method of claim 35, wherein said imaging system includes an optical system.

38. (Previously presented) The method of claim 37, wherein said optical system comprises a microscope and a video camera.

39. (Previously presented) The method of claim 27, wherein said integrated circuit layers are chosen from a group of integrated circuit layers consisting of semiconductor layers, dielectric layers, and photoactive layers.